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EXAMINER	
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2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/610,968	HALL ET AL.	
	Examiner	Art Unit	
	Sudhanshu C. Pathak	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Feb. 20th, 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *18-26* is/are allowed.

6)☒ Claim(s) *1-12,14-17 and 27-29* is/are rejected.

7)☒ Claim(s) *13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *June 30th, 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-to-29 are pending in the application.

Response to Arguments

2. Applicant's arguments, filed in amendment dated Feb. 20th, 2007, with respect to the specification objections have been fully considered and are persuasive. Therefore, the specification objections have been withdrawn.
3. Applicant's arguments, filed in amendment dated Feb. 20th, 2007, with respect to all the claim objections have been fully considered and are not persuasive. Therefore, the applicable claim objections have been maintained.
4. Applicant's arguments, filed in amendment dated Feb. 20th, 2007, with respect to the 101 rejections have been fully considered and are persuasive. Therefore, the 101 rejections have been withdrawn.
5. Applicant's arguments, filed in amendment dated Feb. 20th, 2007, with respect to the 112 (1st, Paragraph) rejections have been fully considered and are persuasive. Therefore, the 112 rejections have been withdrawn.
6. Applicant's arguments, filed in amendment dated Feb. 20th, 2007, with respect to the claim rejections (102 & 103) have been fully considered and are not persuasive. Therefore, the claim rejections have been maintained.

In regards to the specific arguments regarding the "Affidavits or declarations under 37 CFR 1.131", are not persuasive i.e. the affidavit does not meet the requirements of diligence. A Declaration under 37 C.F.R. § 1.131 may be satisfied by an adequate showing of (i) conception prior to the effective data of the reference

and (ii) diligence from just prior to the effective data of the reference until the invention is actually or constructively reduced to practice. A constructive reduction to practice is satisfied by the filing of a patent application.

Furthermore, the examiner has verified the affidavit with a supervisor.

Claim Objections

7. Claim 19 is objected to because of the following:

Claim 19 further discloses the variable(s) "L" & "M" wherein it is not clear as to the type of variable "L" & "M" is. It is recommended to amend the claim such as "...where L is an integer" and "...where M is an integer".

8. Claim 24 is objected to because of the following:

Claim 24 discloses the variable "P", however it is not clear as the type of variable "P" represents. It is recommended to amend the claim such as "...where P is an integer...".

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1-2, 4-6, 9-10, 28-29 (method) & 11-12, 14-17 (device) are rejected under 35 U.S.C. 102(a) as being anticipated by Nieczyporowicz et al. (PG PUB 2002/0097703 A1).

In regards to Claim 1, Nieczyporowicz discloses a pseudo-noise (PN) code hopping method for mitigating cross-correlation interference (Abstract, lines 1-9 & Specification, Paragraph 9, lines 1-16), the method comprising the steps of: providing a memory device (Specification, Paragraph 10, lines 4-6 & Specification, Paragraph 83, lines 3-4, 9-11 & Fig. 8, element 50); storing a plurality of orthogonal PN codes in the memory device (Paragraph 7, lines 13-19 & Paragraph 28, lines 9-10 & Paragraph 36, lines 7-10 & Paragraph 81, lines 6-7 & Paragraph 83, lines 1-9 & Fig. 9, elements 60-62 & Fig. 6) {Interpretation: The reference discloses storing a plurality orthogonal PN codes in memory}; pseudo-randomly accessing the memory device to retrieve one of the plurality of PN codes, wherein each of the plurality of PN codes is associated with a useful life cycle before another PN code is pseudo-randomly retrieved (Abstract, lines 6-14, 22-25 & Paragraph 9, lines 1-5 & Paragraph 81, lines 22-24) {Interpretation: The reference discloses performing code-hopping pseudo-randomly i.e. selecting (retrieving) codes pseudo-randomly. Furthermore, the reference discloses a code is selected for a duration of period such as block of symbols or a symbol-by-symbol basis i.e. this is the useful life cycle of the codes}; and spreading a modulated data signal with the retrieved one of the plurality of PN codes (Fig. 9, elements 60-66 & Paragraph 83, lines 13-14).

In regards to Claim 2, Nieczyporowicz discloses a PN code hopping method for mitigating cross-correlation interference as described above. Nieczyporowicz further discloses step of storing the plurality of orthogonal PN codes in the memory device further comprises the steps of: storing unbalanced orthogonal PN codes in the

memory device; and storing balanced orthogonal PN codes in the memory device (Paragraph 7, lines 12-20 & Fig. 6) {Interpretation: The reference discloses storing multiple PN codes including balanced and unbalanced. Furthermore, the number of the type of PN codes stored is a matter of design choice}.

In regards to Claim 4, Nieczyporowicz discloses a PN code hopping method for mitigating cross-correlation interference as described above. Nieczyporowicz further discloses the step of pseudo-randomly accessing the memory device to retrieve one of the plurality of PN codes further comprises the steps of: providing an addressable multiplexer (Fig. 9, element 64); coupling the addressable multiplexer to the memory device ((Paragraph 9, lines 1-5 & Paragraph 10, lines 4-6 & Paragraph 82, lines 1-11 & Fig. 9, elements 60, 62 & Fig. 8, element 50) {Interpretation: The reference discloses storing the PN codes in a table in memory}; clocking a PN-code from the memory device to the addressable multiplexer (Paragraph 83, lines 9-16) {Interpretation: The address generator which can be implemented in memory is clocked at the hopping rate so as to output the spreading codes}; pseudo-randomly selecting an input address of the addressable multiplexer; and outputting from the multiplexer a PN-code associated with the selected input address (Fig. 9, elements 60-64, "c" & Paragraph 81, lines 22-25 & Paragraph 83, lines 9-13).

In regards to Claim 5, Nieczyporowicz discloses a PN code hopping method for mitigating cross-correlation interference as described above. Nieczyporowicz further discloses the step of clocking the PN-code from the memory device further

comprises the step of clocking the PN-code at a rate equal to a symbol rate (Paragraph 83, lines 14-16).

In regards to Claim 6, Nieczyporowicz discloses a PN code hopping method for mitigating cross-correlation interference as described above. Nieczyporowicz further discloses the step of clocking the PN-code from the memory device further comprises the step of clocking the PN-code at a rate equal to an integer multiple of a symbol rate (Abstract, lines 22-25).

In regards to Claim 9, Nieczyporowicz discloses a PN code hopping method for mitigating cross-correlation interference as described above. Nieczyporowicz further discloses the useful lifecycle comprising "N" symbol periods (Abstract, lines 22-25) {Interpretation: The useful lifecycle is analogous to the hopping rate i.e. the duration of time a certain PN code is selected, before hopping}.

In regards to Claim 10, Nieczyporowicz discloses a PN code hopping method for mitigating cross-correlation interference as described above. Nieczyporowicz further discloses the step of spreading the modulated data signal with the retrieved one of the plurality of PN codes further comprises the steps of: spreading a phase shift keying (PSK) modulated signal with the retrieved one of the plurality of PN codes for the useful life cycle associated with the retrieved one of the plurality of PN codes (Paragraph 29, lines 9-11 & Paragraph 51, lines 1-4 & Fig. 9, elements 60, 64-66).

In regards to Claim 11, Nieczyporowicz discloses a pseudo-noise (PN) code hopping device (Fig. 9, elements 60-64), the device comprising: at least one memory device, wherein the at least one memory device comprises: a plurality of time limited

PN codes (Paragraph 9, lines 1-5 & Paragraph 10, lines 4-6 & Paragraph 82, lines 1-11 & Fig. 9, element 60 & Fig. 8, element 50) {Interpretation: The reference discloses storing the PN codes in a table in memory}; an addressable multiplexer (Fig. 9, elements 64), wherein the addressable multiplexer is coupled to the at least one memory device (Fig. 9, elements 60) {Interpretation: The reference discloses the multiplexer is coupled to the plurality of PN codes which are stored in memory}; and an address generator, wherein the address generator is coupled to the addressable multiplexer (Fig. 9, element 62).

In regards to Claim 12, Nieczyporowicz discloses a PN code hopping device for mitigating cross-correlation interference as described above. Nieczyporowicz further discloses the at least one memory device further comprises: a N x SF storage capacity where N = number of chips and SF = N / symbol; and N-parallel outputs (Fig. 9, element 60 & Paragraph 83, line 12 & Paragraph 85, lines 1-9 & Paragraphs 86-87) {Interpretation: The reference discloses the memory capacity to be P chips / symbol which is number of chips / symbol "by" nP wherein if "n" a variable is 1 then P is the number of chips. Furthermore, the memory has "nP" parallel outputs of which any one is selected as is shown in Fig. 9. Therefore, the variable "P" is analogous to variable "N"}.

In regards to Claim 14, Nieczyporowicz discloses a PN code hopping device for mitigating cross-correlation interference as described above. Nieczyporowicz further discloses the addressable multiplexer comprises a N:I multiplexer where N number of chips associated with one of the plurality of time limited PN codes (Fig. 9, element

64 & Paragraph 83, lines 12-13) {Interpretation: The reference discloses the multiplexer comprising "nP" inputs wherein nP is the number of chips and 1 output}.

In regards to Claim 15, Nieczyporowicz discloses a PN code hopping device for mitigating cross-correlation interference as described above. Nieczyporowicz further discloses the address generator comprises a look-up-table (LUT) (Fig. 8, element 50 & Fig. 9, element 60 & Paragraph 81, lines 6-15) {Interpretation: The reference discloses storing the PN codes in a look up table}.

In regards to Claim 16, Nieczyporowicz discloses a PN code hopping device for mitigating cross-correlation interference as described above. Nieczyporowicz further discloses the address generator comprises a shift generator (Paragraph 83, lines 9-11 & Paragraph 7, lines 11-13) {Interpretation: The reference discloses the address generator implemented with a linear feedback shift register (LFSR)}.

In regards to Claim 17, Nieczyporowicz discloses a PN code-hopping device for mitigating cross-correlation interference as described above. Nieczyporowicz further discloses the address generator comprises an up-down counter (Paragraph 83, lines 16-22 & Fig. 8, element 50 & Fig. 9, element 60 & Paragraph 81, lines 6-15) {Interpretation: The reference discloses storing the PN codes in a look up table}.

In regards to Claim 28, Nieczyporowicz discloses A PN code hopping method for mitigating cross- correlation interference (Abstract, lines 1-9 & Specification, Paragraph 9, lines 1-16), the method comprising the steps of: providing a first set of PN spreading codes, the first set of PN spreading codes comprising: a first subset of hoppable PN codes; a second subset of non-hoppable PN codes, wherein the

second subset of non-hoppable PN codes is used for system control purposes, the second subset of non-hoppable PN codes comprising: at least one PN spreading code (Abstract, lines 14-20) {Interpretation: The reference discloses two subset of codes i.e. a hopped subset and a non-hopped subset wherein the non-hopped codes are used for control channels wherein each subset has plurality of codes}; providing a memory device (Specification, Paragraph 10, lines 4-6 & Specification, Paragraph 83, lines 3-4, 9-11 & Fig. 8, element 50); storing the first set of PN codes in the memory device (Paragraph 7, lines 13-19 & Paragraph 28, lines 9-10 & Paragraph 36, lines 7-10 & Paragraph 81, lines 6-7 & Paragraph 83, lines 1-9 & Fig. 9, elements 60-62 & Fig. 6) {Interpretation: The reference discloses storing a plurality orthogonal PN codes in memory}; pseudo-randomly accessing the memory device to retrieve one of the first subset of hoppable PN codes (Abstract, lines 6-14, 22-25 & Paragraph 9, lines 1-5 & Paragraph 81, lines 22-24) {Interpretation: The reference discloses performing code-hopping pseudo-randomly i.e. selecting (retrieving) codes pseudo-randomly}; spreading a modulated data signal with the retrieved one of the first subset of hoppable PN codes (Fig. 9, elements 60-66 & Paragraph 83, lines 13-14).

In regards to Claim 29, Nieczyporowicz discloses a PN code hopping method for mitigating cross-correlation interference as described above. Nieczyporowicz further discloses the step of spreading the modulated data signal further comprises the step of spreading the modulated data for a time substantially equal to an integer multiple of a symbol time (Abstract, lines 11-14, 22-25 & Paragraph 9, lines 1-5 & Fig. 9,

element 66) {Interpretation: The reference discloses spreading data with a specified PN code, wherein the PN code is varied over time substantially equal to an integer multiple of a symbol time, therefore, the data is spread for a time substantially equal to an integer multiple of a symbol time}.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nieczyporowicz et al. (PG PUB 2002/0097703 A1) in view of Jones et al. (5,696,789).

In regards to Claim 3, Nieczyporowicz discloses a PN code hopping method for mitigating cross-correlation interference as described above. However, Nieczyporowicz does not disclose the step of storing unbalanced orthogonal PN codes in the memory device further comprises the step of storing Gold PN codes.

Jones discloses implementing a spread spectrum communication system comprising orthogonal codes consisting of Gold codes (Abstract, lines 1-5 & Column 7, lines 24-40). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention that Jones discloses implementing Gold codes as a PN code and this is implemented in the method as described in Nieczyporowicz so

as to provide an orthogonal code for mitigating interference which are simple to implement, thus reducing the complexity of the code generator.

13. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nieczyporowicz et al. (PG PUB 2002/0097703 A1) in view of Henry at al. (PG PUB 2003/0154223 A1).

In regards to Claims 7-8, Nieczyporowicz discloses a PN code hopping method for mitigating cross-correlation interference as described above. However, Nieczyporowicz does not disclose the step of pseudo- randomly selecting an input address of the addressable multiplexer further comprises the step of constraining the pseudo-random selection to select the input address based upon a previously selected one of the plurality of PN codes.

Henry discloses a pseudo random number generator implemented in software wherein the initial seed value is selected by the user to generate the first random result, which is then used to seed the generator to generate the second random result (Paragraphs 14-15) {Interpretation: The reference discloses the implementation of a pseudo-random number generator which is analogous to the claimed limitation in the application of PN codes, wherein the present output is based on the previous output}. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Henry discloses a pseudo-random generator and this is implemented in the method as described in Nieczyporowicz so as to implement a PN code generator in the software domain this minimizing the hardware components of the code generator and is implemented on

a processor so as to be able to reduce the size of the transceiver and furthermore provide flexibility of implementing modifications by changing the programming instructions and seed value. Furthermore, there is no criticality in selecting the previous selected input address or the previously selected PN code, this is a matter of design choice, and since both the address value also represents a PN code.

14. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nieczyporowicz et al. (PG PUB 2002/0097703 A1) in view of Callaway (6,922,432).

In regards to Claim 27, Nieczyporowicz discloses a pseudo-noise (PN) code hopping method for mitigating cross- correlation interference (Abstract, lines 1-9 & Specification, Paragraph 9, lines 1-16), the method comprising the steps of: providing a memory device (Specification, Paragraph 10, lines 4-6 & Specification, Paragraph 83, lines 3-4, 9-11 & Fig. 8, element 50); storing a plurality of orthogonal PN codes in the memory device (Paragraph 7, lines 13-19 & Paragraph 28, lines 9-10 & Paragraph 36, lines 7-10 & Paragraph 81, lines 6-7 & Paragraph 83, lines 1-9 & Fig. 9, elements 60-62 & Fig. 6) {Interpretation: The reference discloses storing a plurality orthogonal PN codes in memory}; pseudo-randomly accessing the memory device to retrieve one of the plurality of PN codes, wherein each of the plurality of PN codes is associated with a useful life cycle before another PN code is pseudo-randomly retrieved (Abstract, lines 6-14, 22-25 & Paragraph 9, lines 1-5 & Paragraph 81, lines 22-24) {Interpretation: The reference discloses performing code-hopping pseudo-randomly i.e. selecting (retrieving) codes pseudo-randomly.

Furthermore, the reference discloses a code is selected for a duration of period such as block of symbols or a symbol-by-symbol basis i.e. this is the useful life cycle of the codes}; and spreading a modulated data signal with the retrieved one of the plurality of PN codes (Fig. 9, elements 60-66 & Paragraph 83, lines 13-14). However, Nieczyporowicz does not disclose a program storage device readable by a computer tangibly embodying a program of instructions executable by the computer to perform the steps of the method.

Callaway discloses a direct sequence spread spectrum (DSSS) communications system comprising a transmitter and a receiver (Fig.'s 1, 9-10 & Column 1, lines 39-67). Callaway further discloses a computer readable medium containing programming instructions for operating a transmitter, the computer readable medium including programming instructions for: obtaining a first direct sequence spread spectrum code; and transmitting the first direct sequence spread spectrum code (Claim 36) {Interpretation: The reference discloses implementing a DSSS system comprising a computer readable medium for obtaining codes and spreading it with data to be transmitted to obtaining a spread signal to transmit}. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention that Callaway teaches a program storage device readable by a computer tangibly embodying a program of instructions executable by the computer to perform the steps of transmitting a spread spectrum signal and this is implemented in the method as described in Nieczyporowicz so as to implement the transmitter and receiver baseband functions on an integrated chip such as a process so as to be

able to reduce the size of the transceiver and furthermore provide flexibility of implementing modifications by changing the programming instructions.

Allowable Subject Matter

15. Claim 13 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

16. Claims 18-26 are allowed over the prior art of record.

17. Claims 18-26 are allowable over the prior art of record because the cited reference do not contain the specified limitation of a pseudo-noise (PN) code hopping System for mitigating cross- correlation interference between Direct Sequence-Code Division Multiple Access (DS-CDMA) users, the system comprising: a first PN code hopping module, wherein the first PN code hopping module comprises: a first memory device; a first addressable multiplexer, wherein the addressable multiplexer is coupled to the first memory device; a first address generator, wherein the first address generator is coupled to the first addressable multiplexer; a second PN code hopping module, the second PN code hopping module is coupled to the first PN code hopping module, wherein the second PN code hopping module comprises: a second memory device; a second addressable multiplexer, wherein the addressable multiplexer is coupled to the second memory device; and a second address generator, wherein the second address generator is coupled to the second addressable multiplexer.

Conclusion

18. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sudhanshu C. Pathak whose telephone number is (571)-272-3038. The examiner can normally be reached on M-F: 9am-6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571)-272-3042.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Sudhanshu C. Pathak
Examiner
Art Unit 2611

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER